

MEMORY READ STROBE PULSE OPTIMIZATION TRAINING SYSTEM

Armen D. Avakian et al.

Docket No. EMC2-159PUS

2/6

FIG. 2

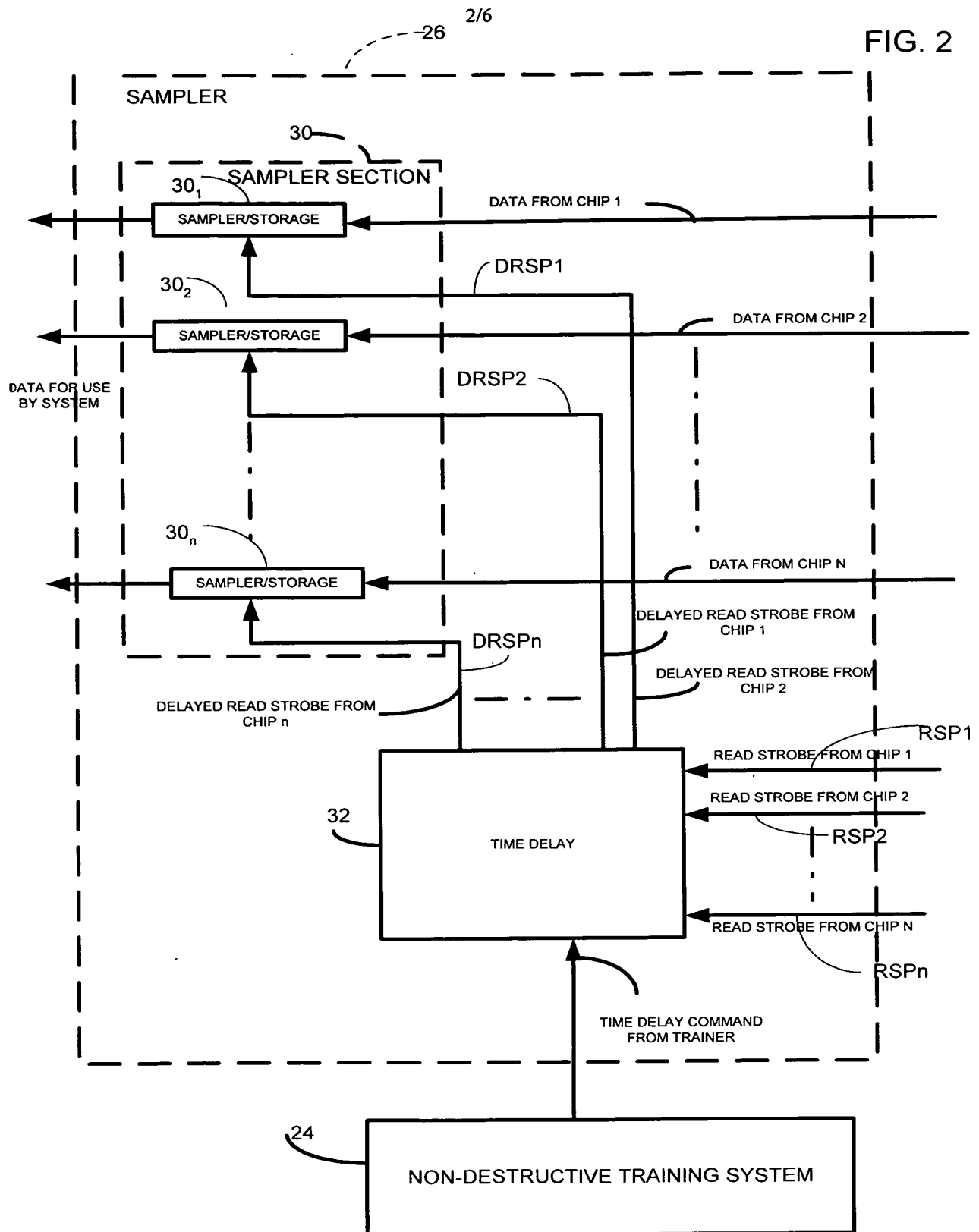
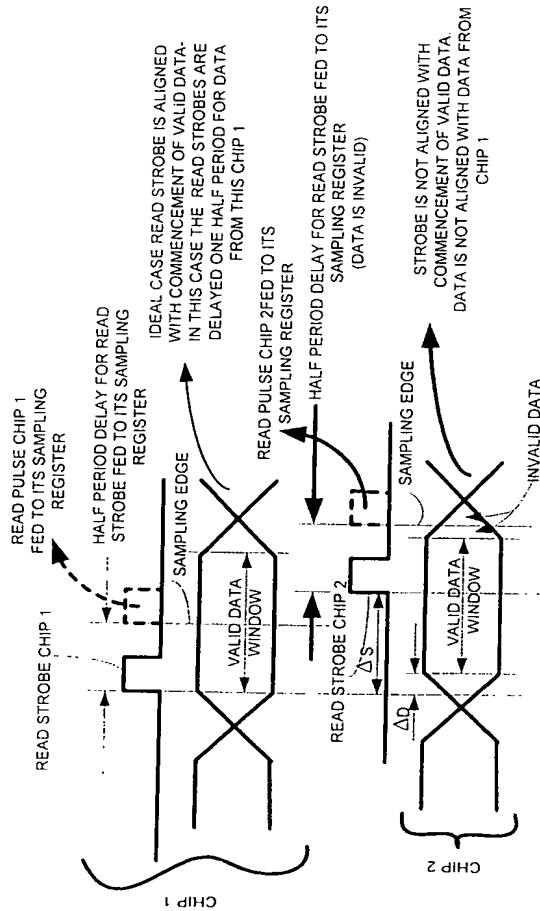
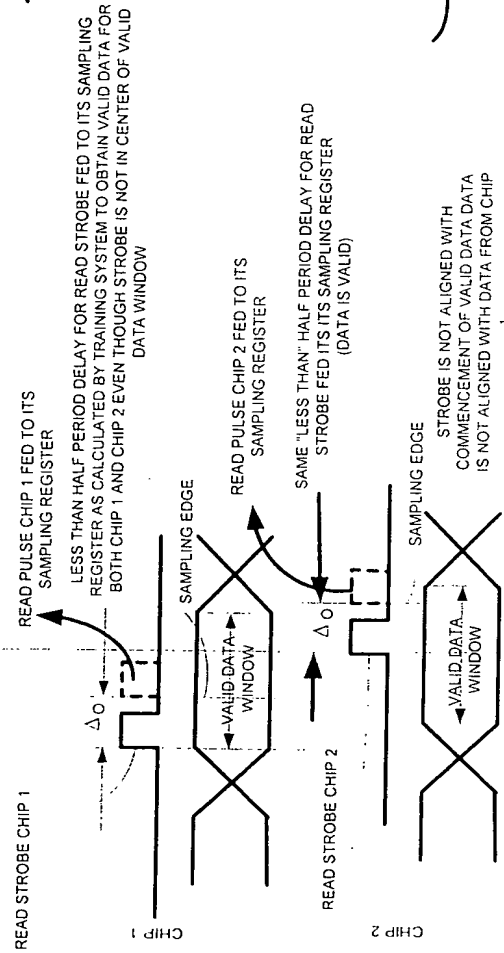


FIG. 2A



WITHOUT TRAINING TO OPTIMIZE DELAY APPLIED TO ALL READ STROBE PULSES WHICH ENABLES INVALID DATA TO BE STORED IN SAMPLING REGISTERS OF BOTH CHIP 1 AND CHIP 2

FIG. 2B



WITH TRAINING TO OPTIMIZE DELAY APPLIED TO ALL READ STROBE PULSES WHICH ENABLES VALID DATA TO BE STORED IN SAMPLING REGISTERS OF BOTH CHIP 1 AND CHIP 2

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4/6

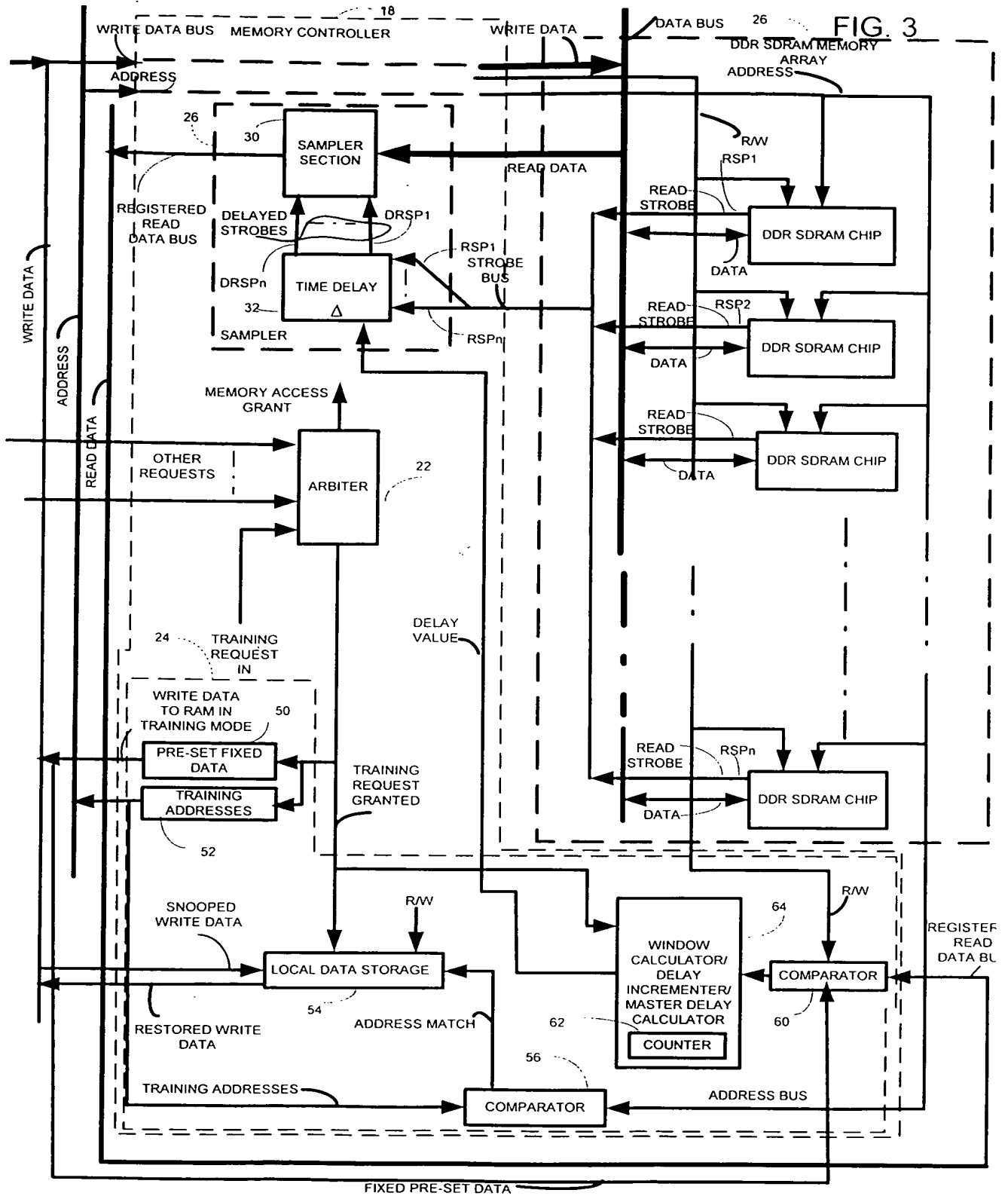


FIG. 4

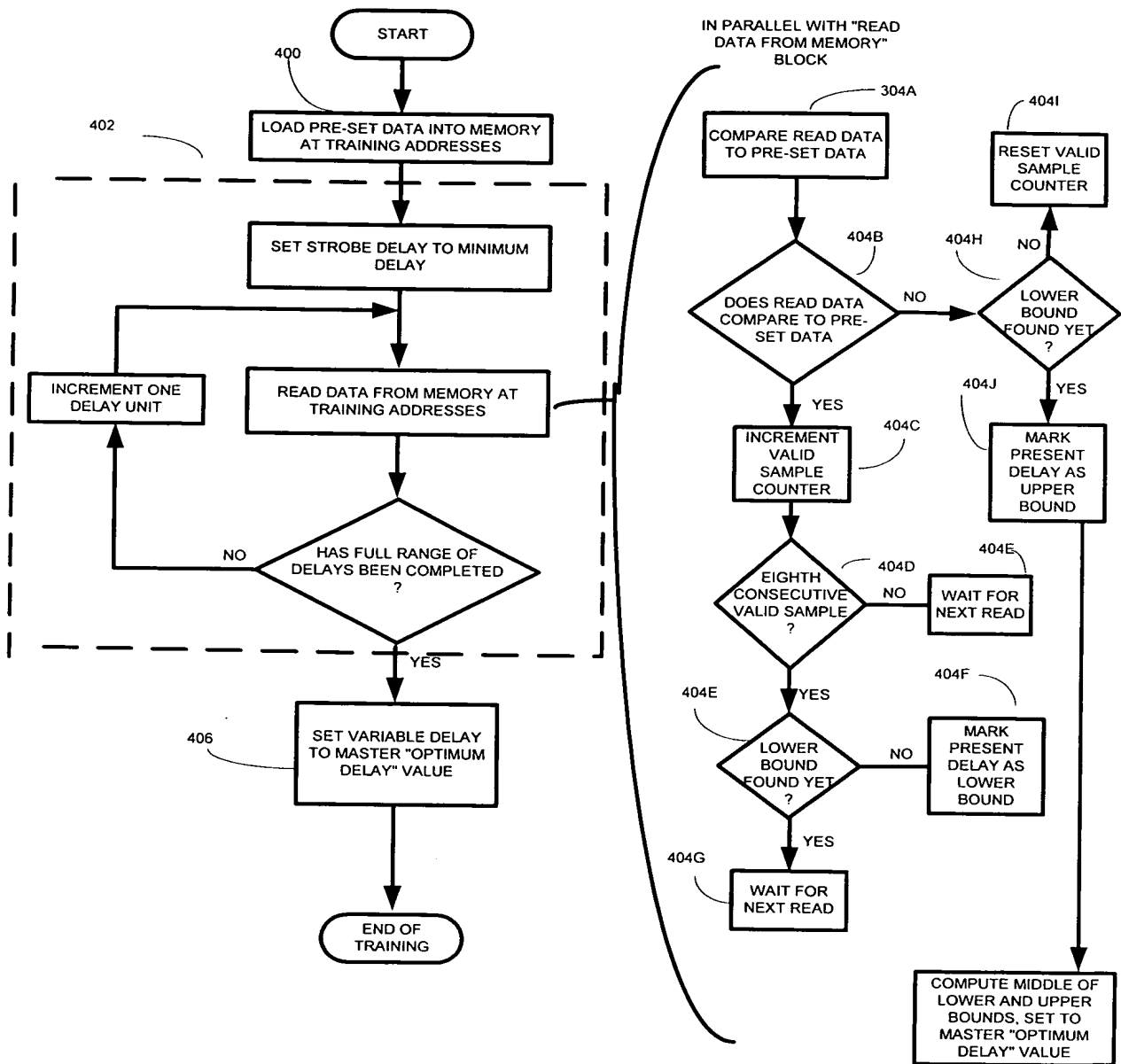


FIG. 5

